MINIMIZING POWER AMPLIFIER MEMORY EFFECTS

ALLEN KATZ* AND MARC FRANCO

*The College Of New Jersey

Linearizer Technology, Inc. ™

3 Nami Lane, Unit C-9 / Hamilton, NJ 08619 / Tel: 609.584.8424 / Fax: 609.631.0177
www.lintech.com

Introduction

- Memory Effects (ME) are changes in a Power Amplifier's (PA) non-linear characteristics resulting from the past history of the input signal.

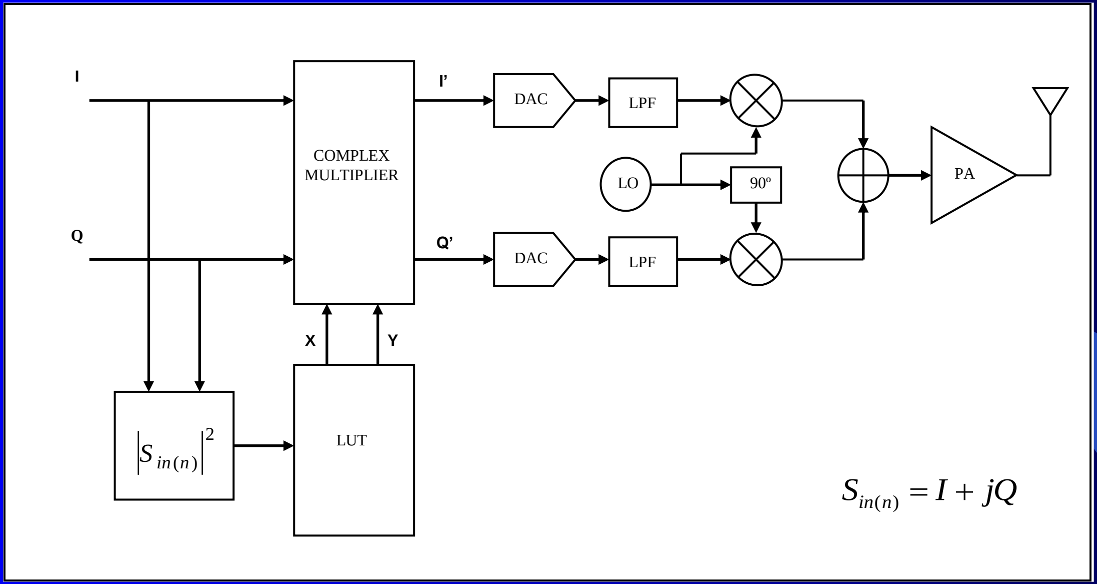
Vo = f(Vin, time)

- Standard predistortion linearization depends on a stable non-linear response, and is particularly degraded by memory effects
- Techniques to reduce PA memory effects will be presented

OUTLINE

- Why minimize memory effects in PA’s ?
- Discuss different sources of ME and how to suppress them
  - Frequency ME
  - Drain/collector ME
  - Gate/base ME
  - Device related ME
  - Thermal ME
- Summarize and conclude

BASIC DSP PREDISTORTION (PD) LINEARIZER

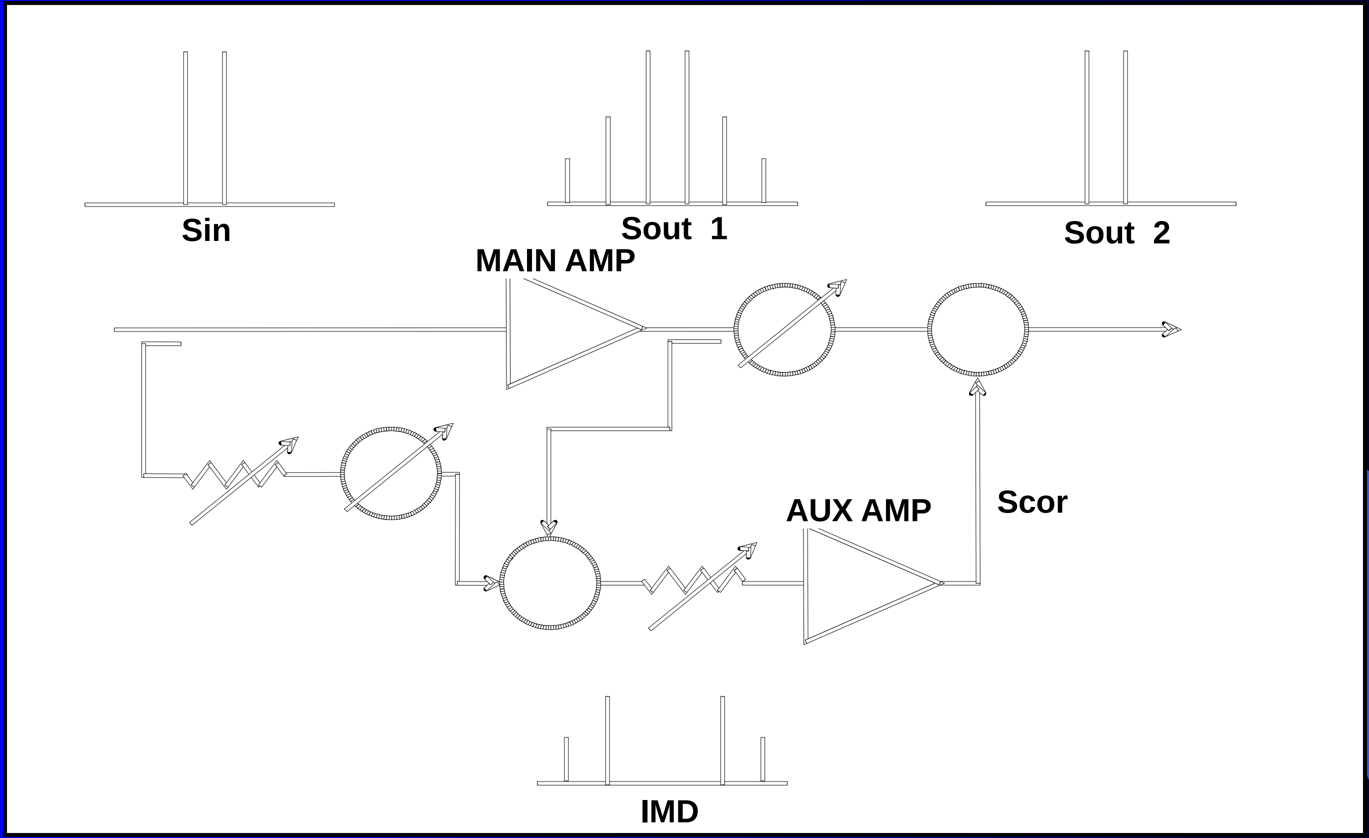


- Every input level has a corresponding output level
- Correction (mag & phase) in look up tables (LUT) depends on input level
- LUT often adaptively updated for slow changes over time

BASIC DSP PREDISTORTION LINEARIZER

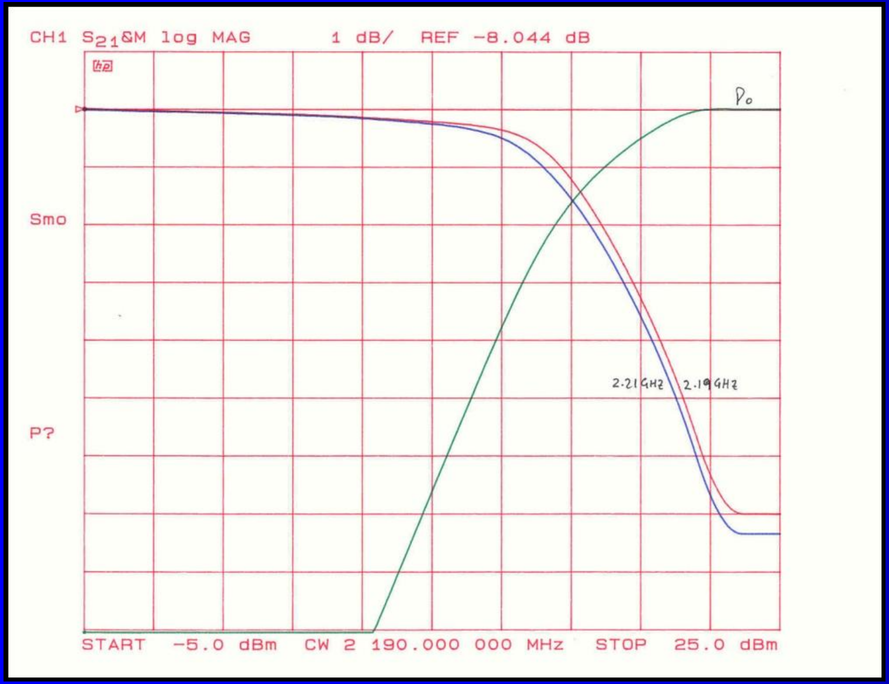
- Memory Effects cause correction to depend on recent past
- If correction depends on additional parameters, system can become very complex (huge multi dimensional LUTs, limited processing time and bandwidth)
- Feedback is not a solution because amplifier time delay limits maximum bandwidth
- Best solution is to minimize ME by PA design

FEEDFORWARD LINEARIZATION

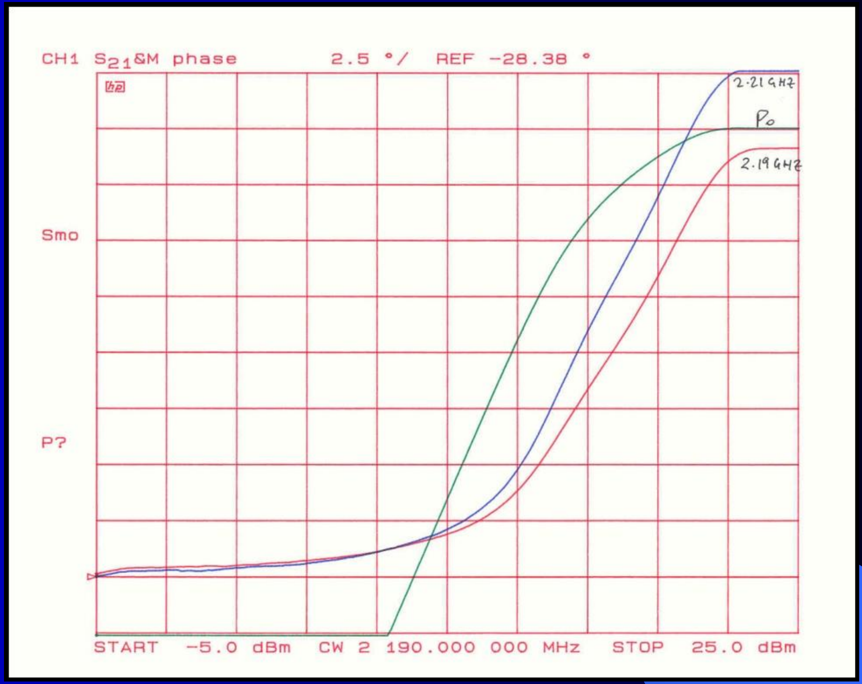


Automatically corrects for memory effects, but is more complex and less efficient than predistortion

FREQUENCY MEMORY EFFECTS



GAIN VS. INPUT POWER IS AFFECTED BY FREQUENCY



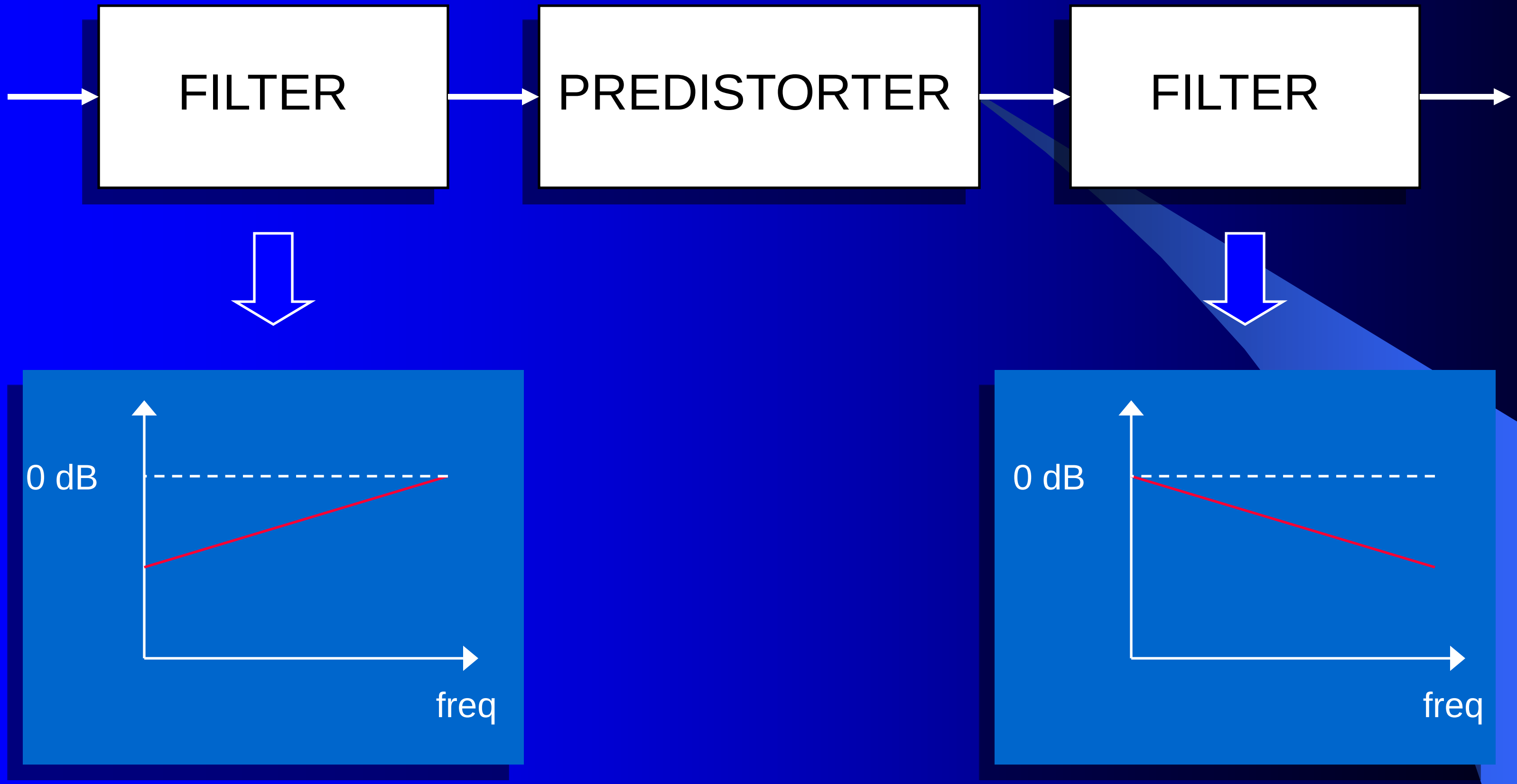
PHASE VS. INPUT POWER IS AFFECTED BY FREQUENCY

- Standard predistorter look-up tables have the same correction for every frequency
- Real PA non-linearities do change with frequency

FREQUENCY MEMORY EFFECTS

- No easy circuit solution for wideband signals
- Design PA for as wide a bandwidth as possible
- Avoid frequency selective components
- Achieve low SWR at input and output and maintain it low across full band of interest
- Must equalize small signal gain and phase to achieve good wideband performance
- Adaptive techniques can correct for frequency changes of limited bandwidth signals

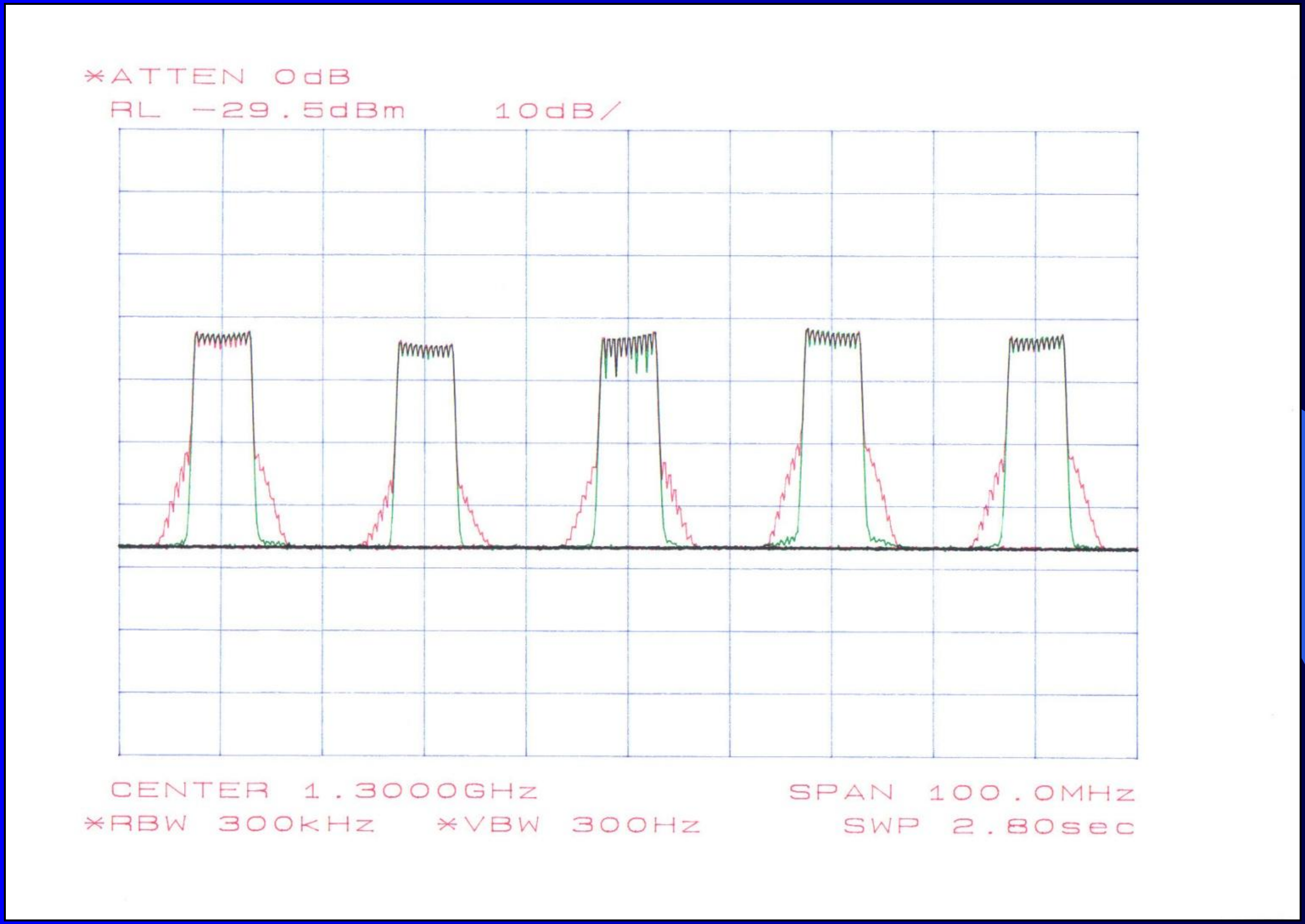
FREQUENCY MEMORY EFFECTS



FILTER → PREDISTORTER → FILTER

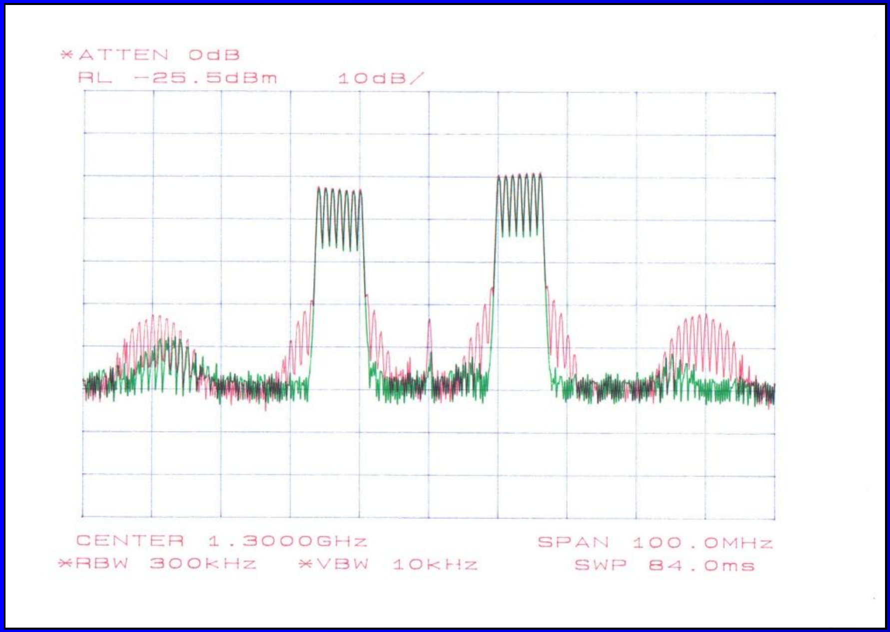
Proposed architecture for reducing memory effects produced by frequency sensitivity

FREQUENCY MEMORY EFFECTS

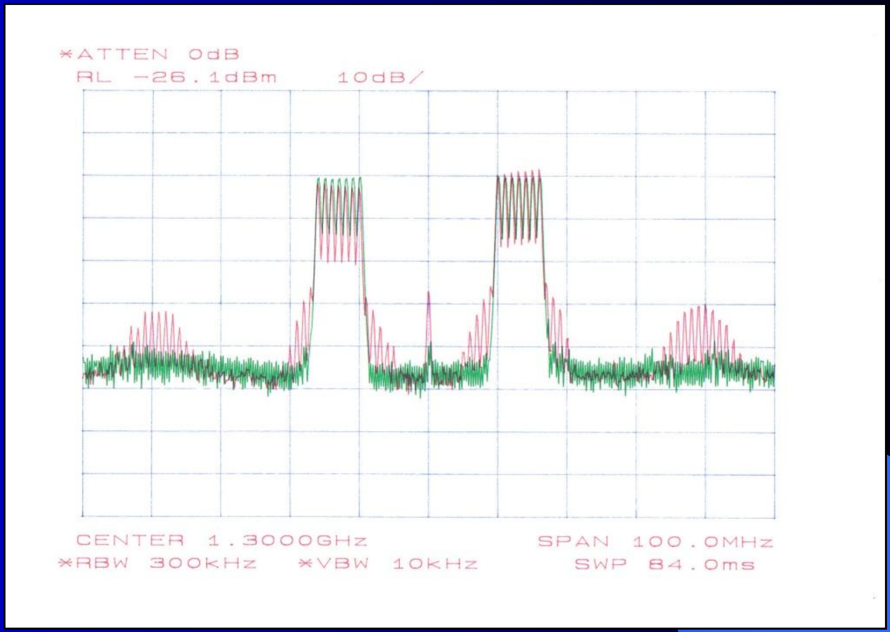


Digital linearization across 100 MHz using filters to correct for frequency memory effects

FREQUENCY MEMORY EFFECTS



Digital linearization across 100 MHz without memory effects correction

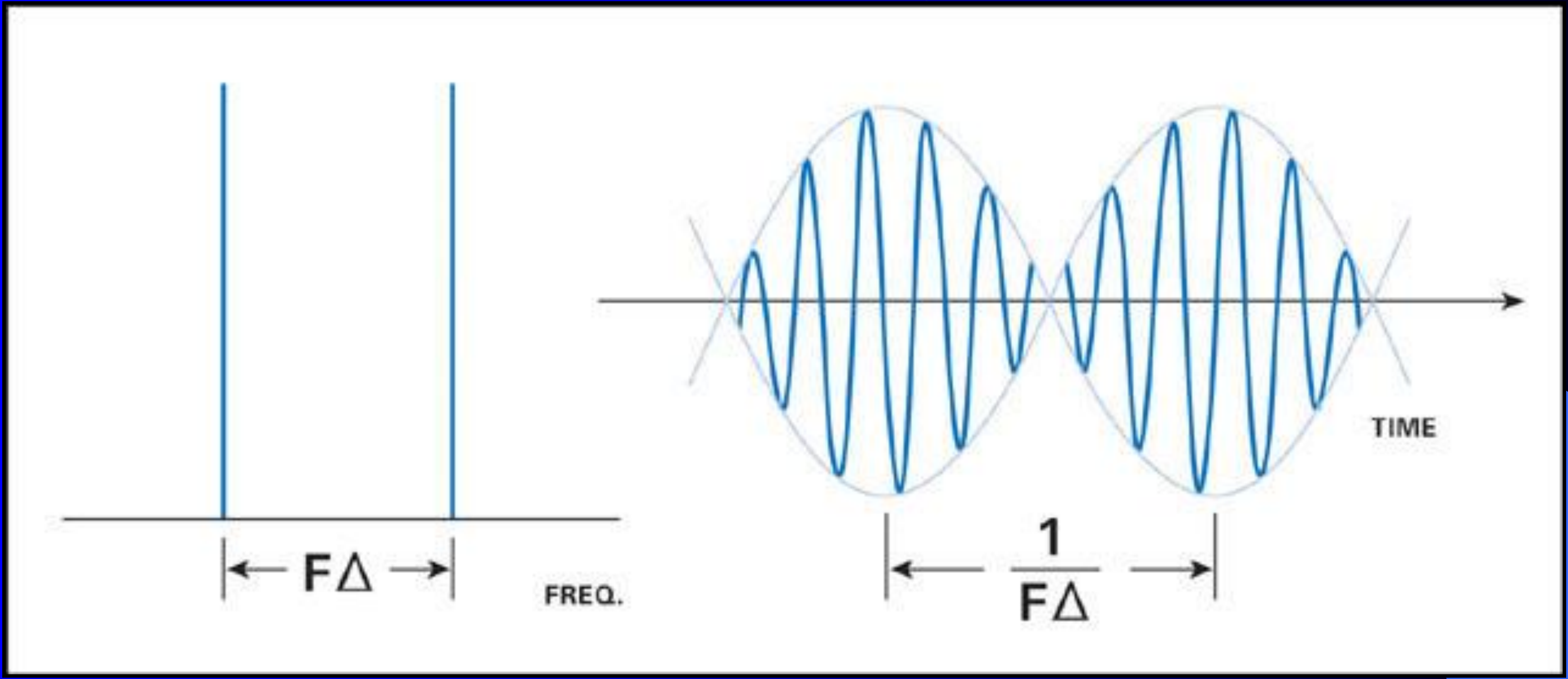


Digital linearization across 100 MHz with memory effects correction

DRAIN/COLLECTOR MEMORY EFFECTS

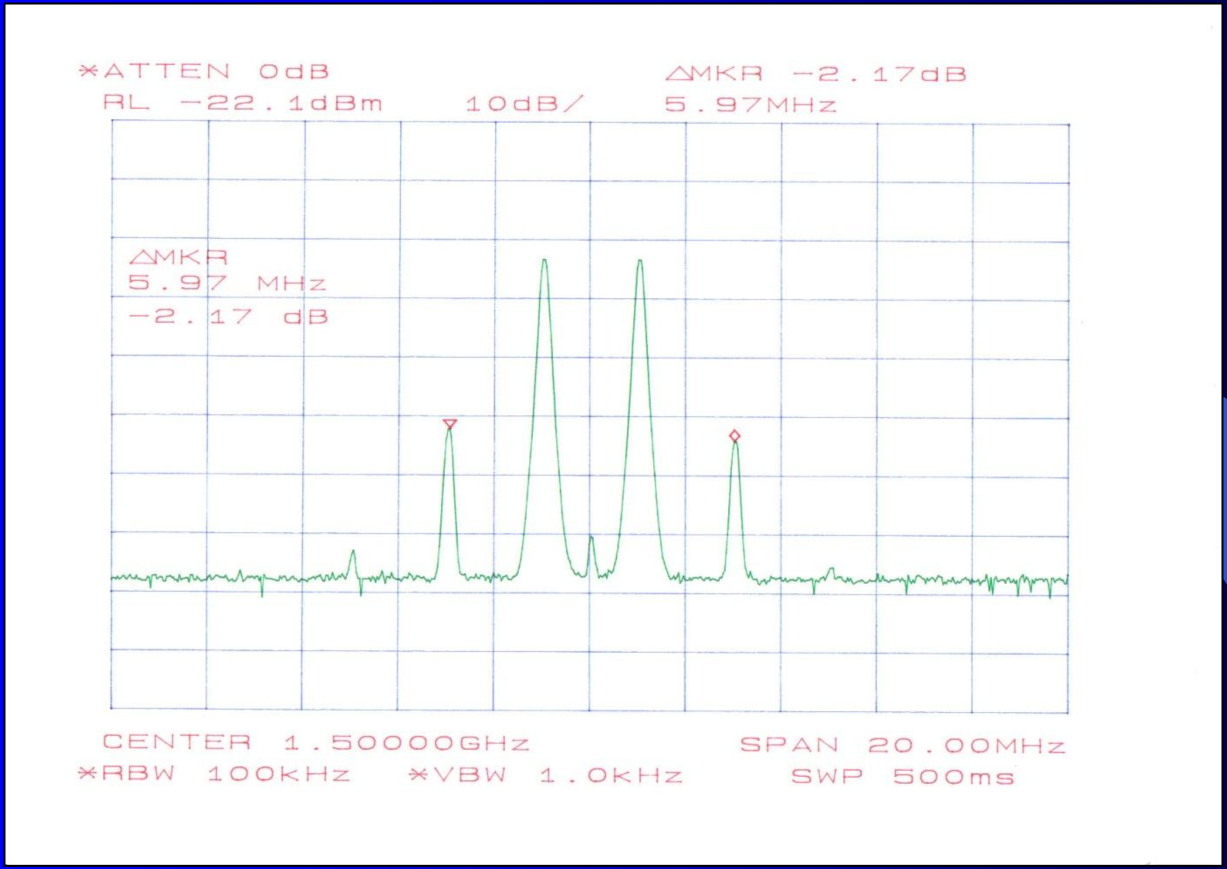
- The major contributor to ME in many PAs is change in drain (or collector) voltage due to non-zero bias/power supply impedance
- All PAs must isolate the RF (i.e. microwave) signal from the dc power supply
- The drain isolation circuit must have a low impedance at the signal’s baseband (envelope) frequencies, to avoid envelope dependent voltage changes at the drain
- Even class A PAs will have an envelope dependent voltage change, although the problem becomes worse as a PA’s bias moves toward class B

DRAIN/COLLECTOR MEMORY EFFECTS



Change in drain voltage amplitude modulates and phase modulates the PA output producing sidebands at the same frequencies as intermodulation distortion (IMD)

IMD NON-SYMMETRY



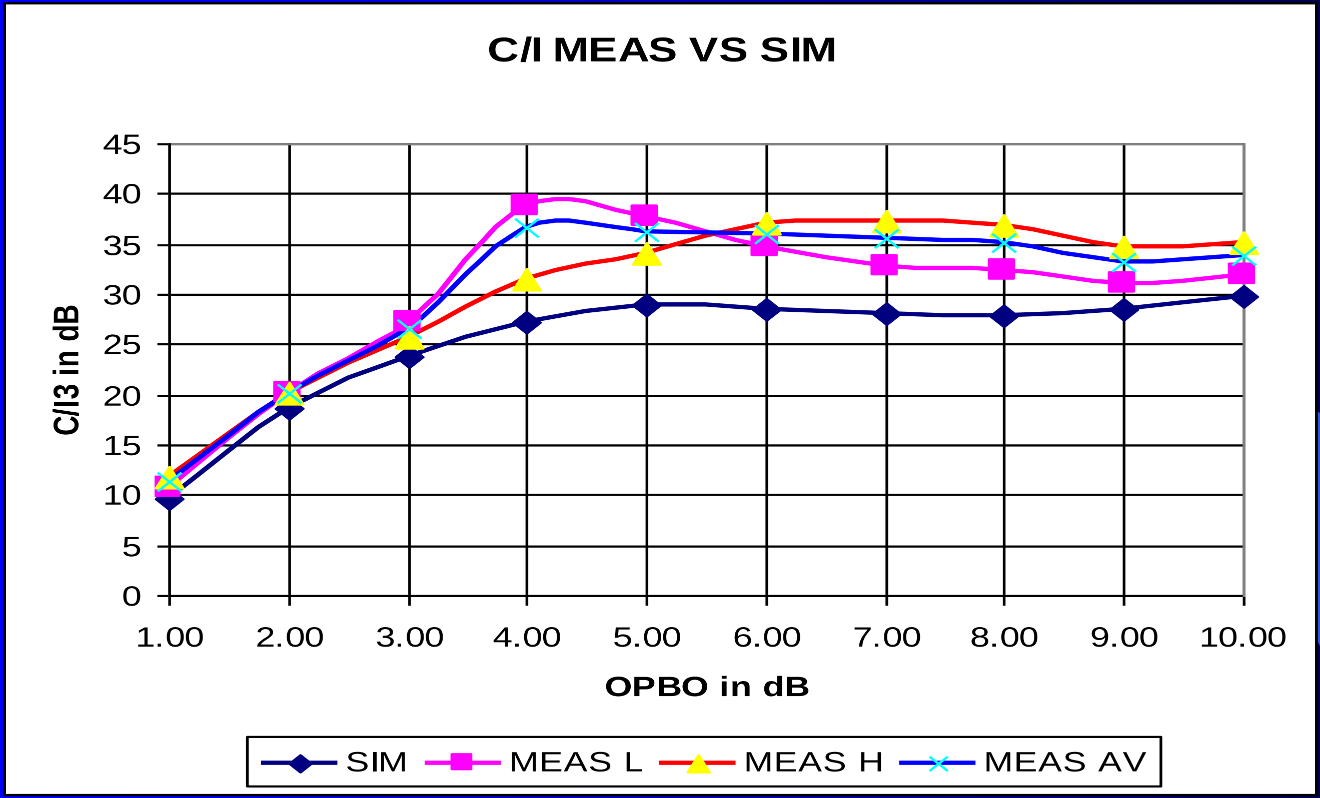
*ATTEN 0dB
RL −22.1dBm 10dB/
ΔMKR −2.17dB
5.97MHz

ΔMKR
5.97 MHz
−2.17 dB

CENTER 1.50000GHz
*RBW 100kHz *VBW 1.0kHz
SPAN 20.00MHz
SWP 500ms

Non-symmetrical IMD products can result from the interaction of device and drain / gate ripple induced IMD
(simplest test for PA memory effects)

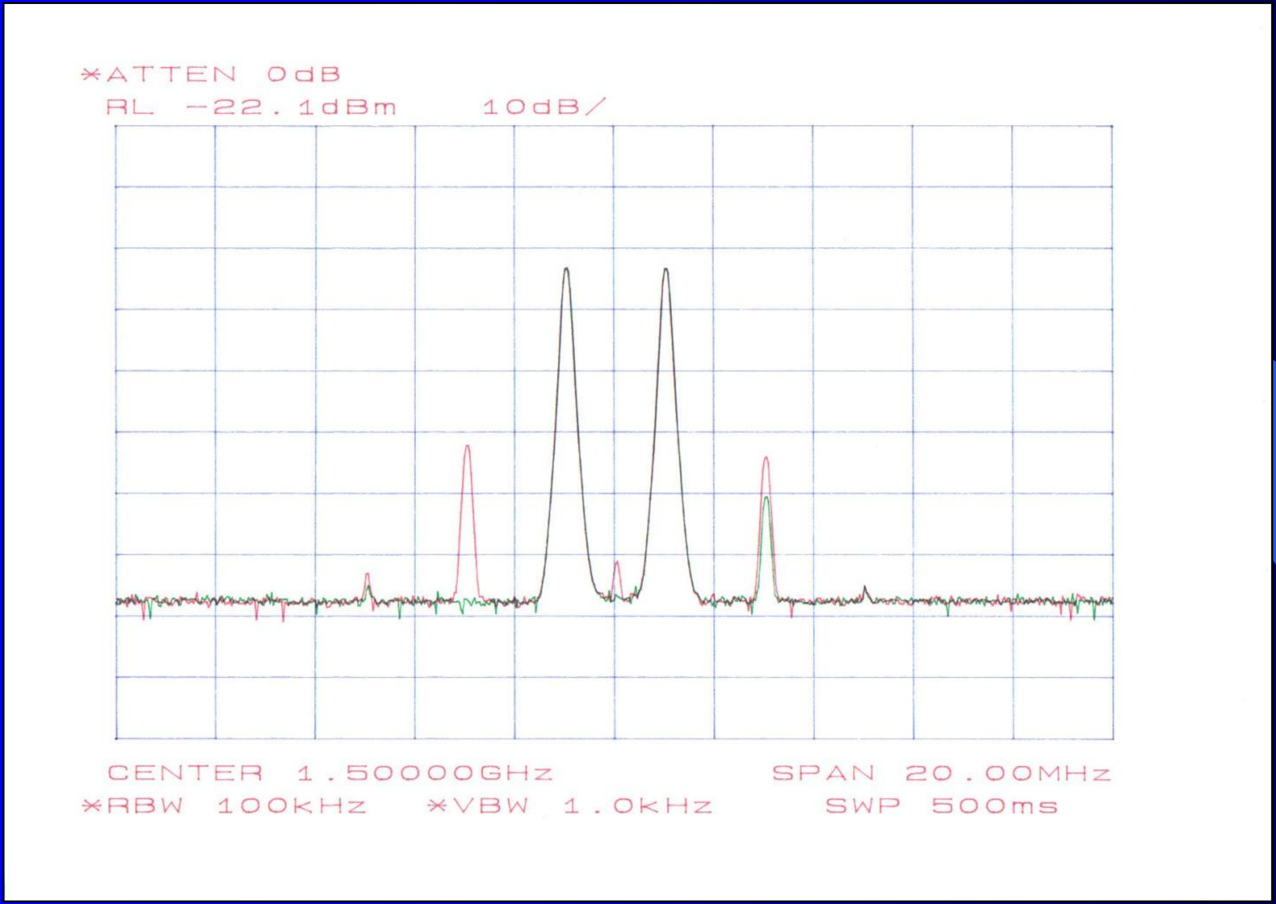
IMD NON-SYMMETRY



Overall carrier to interference (C/I) ratio can be higher than expected based on the PA transfer characteristics

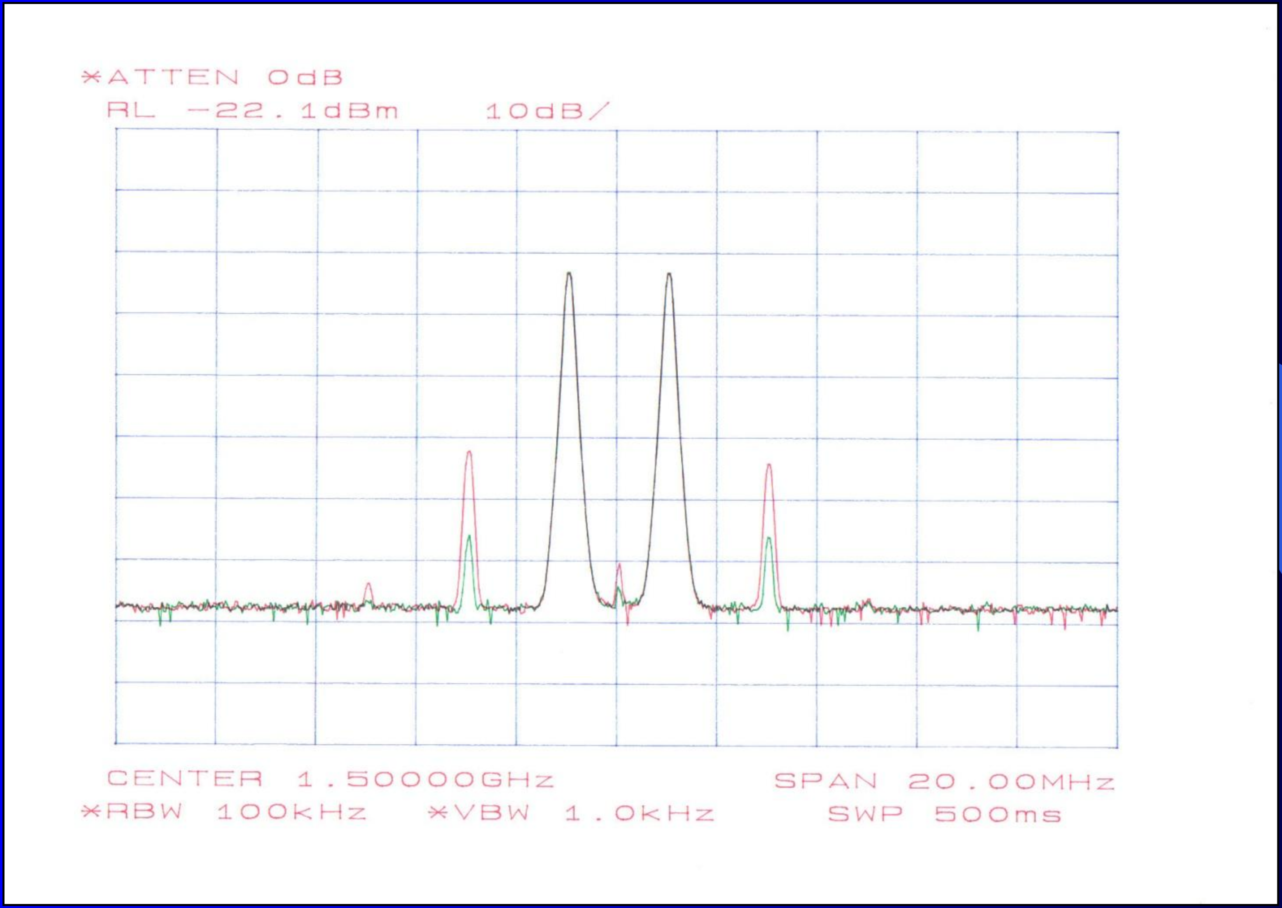
This effect is the result of IMD cancellation

IMD NON-SYMMETRY



Memory effects produce non-even cancellation of IMD

IMD NON-SYMMETRY

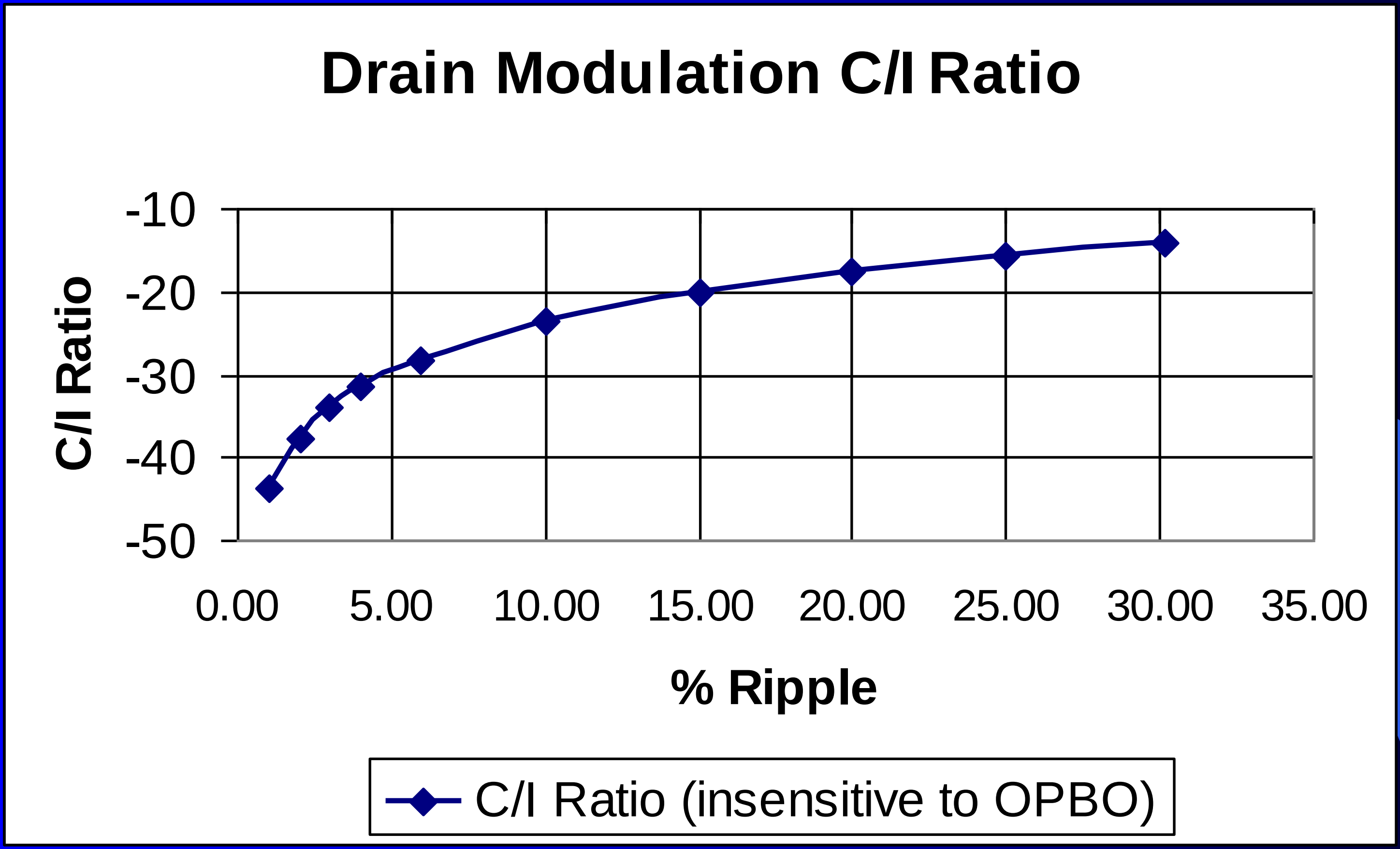


Compromise IMD cancellation can be achieved, but may not be sufficient

RF ENVELOPE (GREEN) IS ~ 140º OUT OF PHASE WITH DRAIN RIPPLE (YELLOW)

IMDs caused by the PA non-linearity subtract from the ripple induced IMDs

DRAIN/COLLECTOR MEMORY EFFECTS



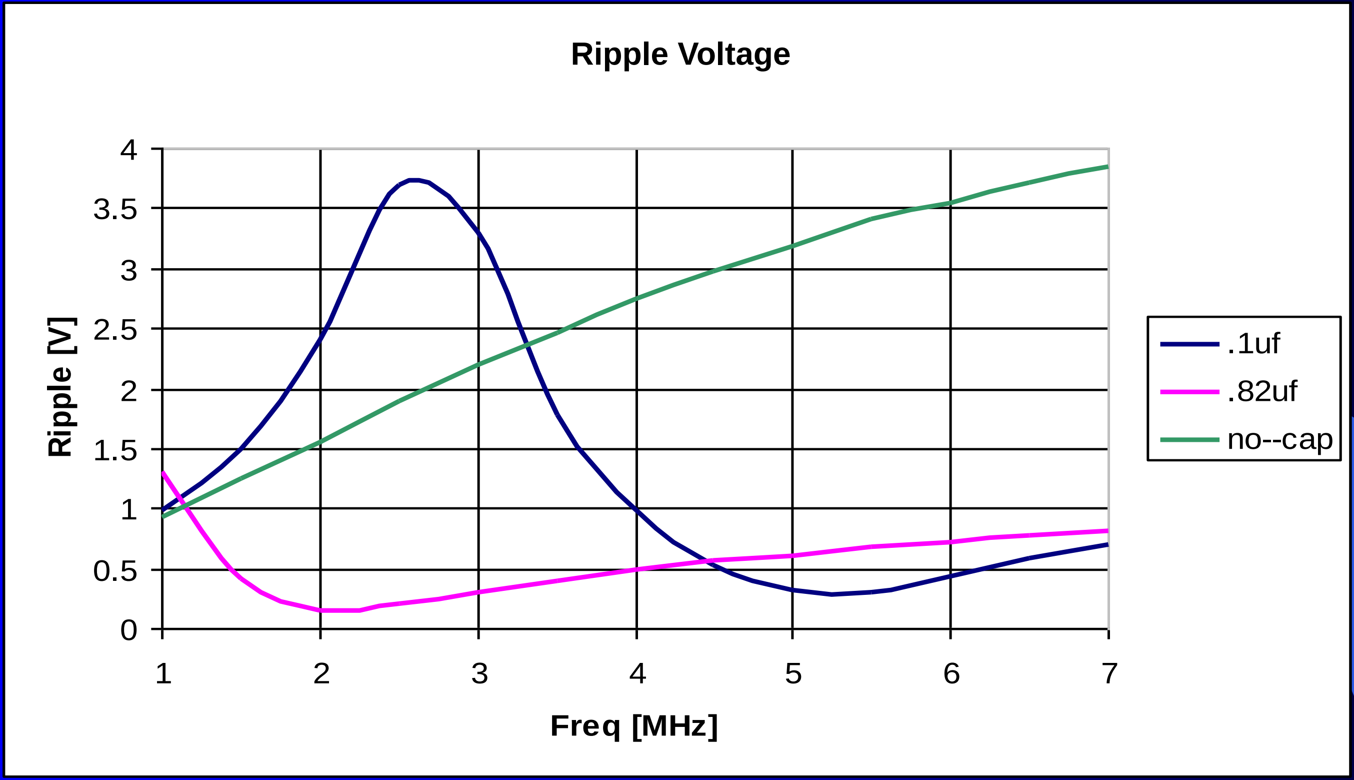
Measurement of the sensitivity of a GaAs FET PA to drain modulation

Ripple < 2% is required for C/I < 40 db

DRAIN/COLLECTOR MEMORY EFFECTS

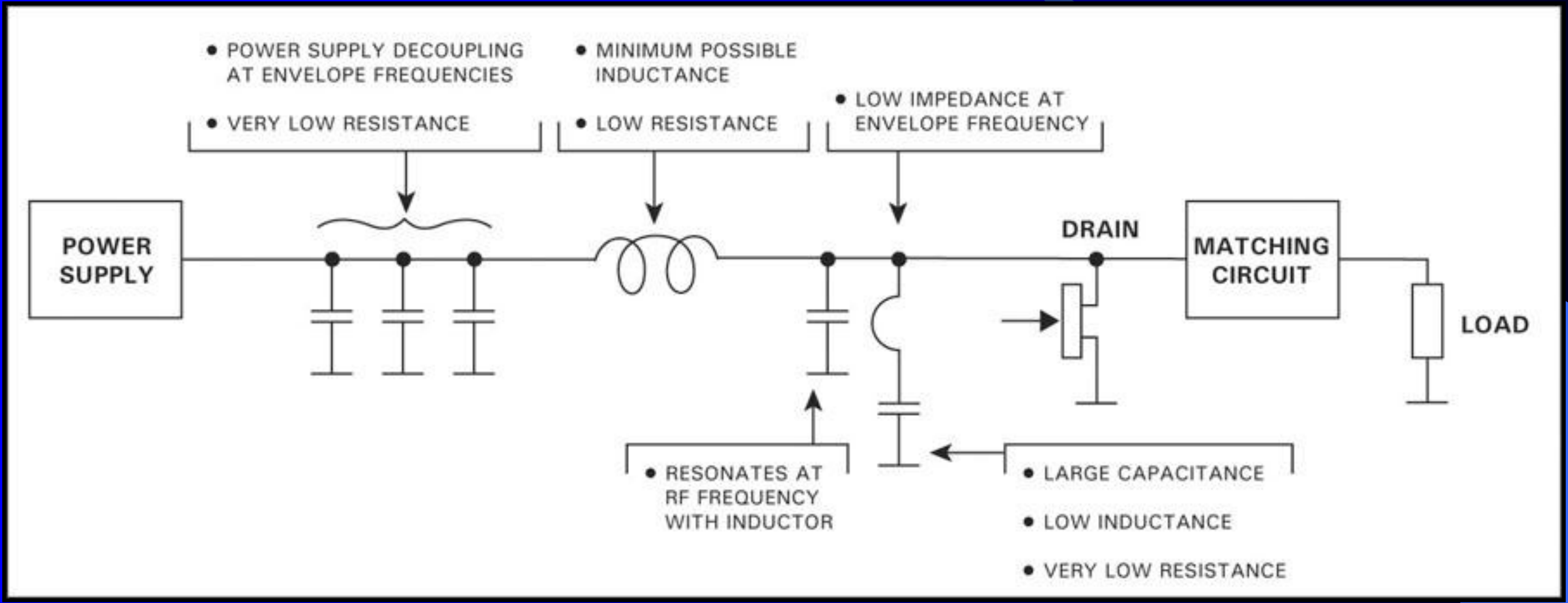
Amplifier linearity can change and often degrades with increasing carrier spacing

DRAIN/COLLECTOR MEMORY EFFECTS



- For wide or even moderate bandwidth signals, the drain ripple is not a trivial problem
- Consider a 250 MHz PA with a 25 MHz multi carrier signal

DRAIN/COLLECTOR MEMORY EFFECTS MINIMIZATION

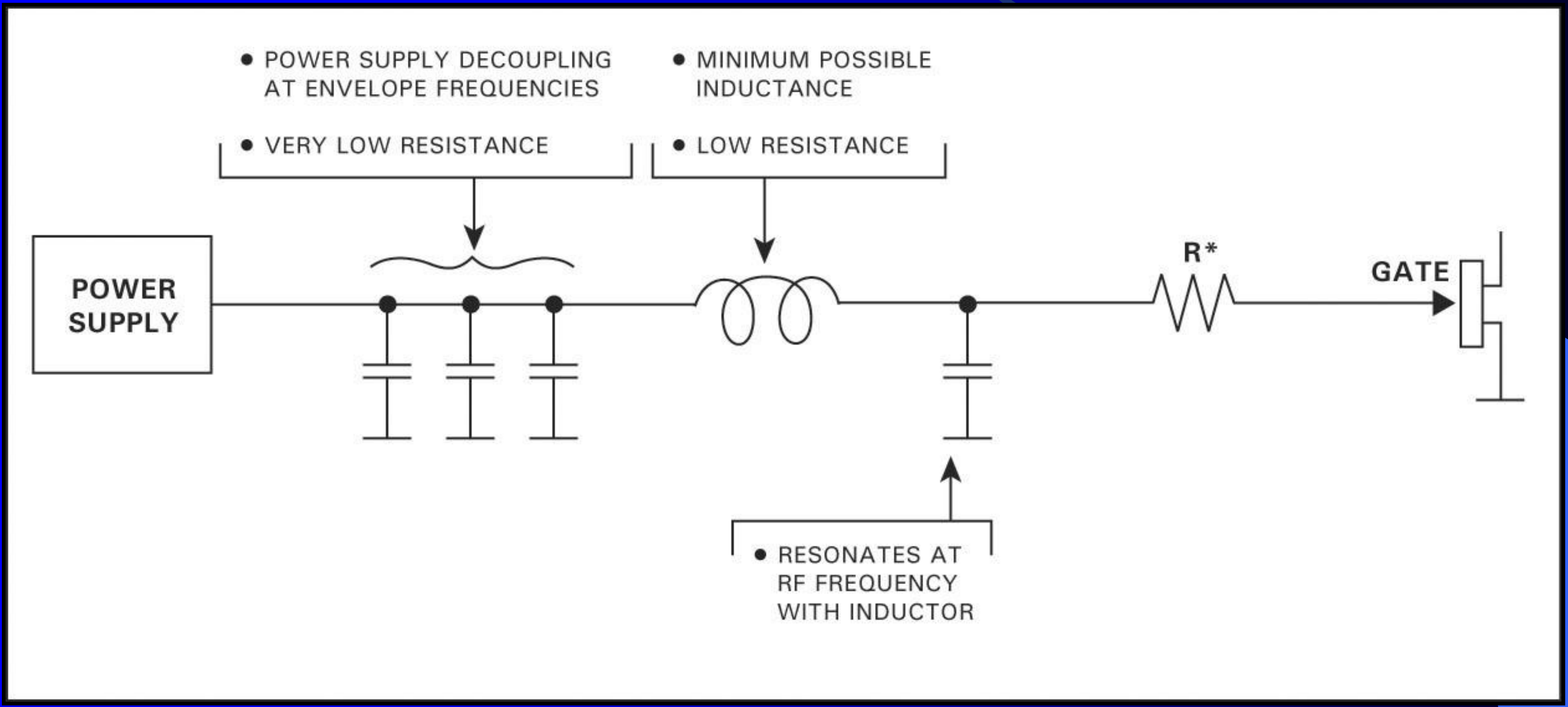


A low impedance network at envelope frequencies across the drain and effective power supply decoupling can minimize memory effects

GATE/BASE MEMORY EFFECTS

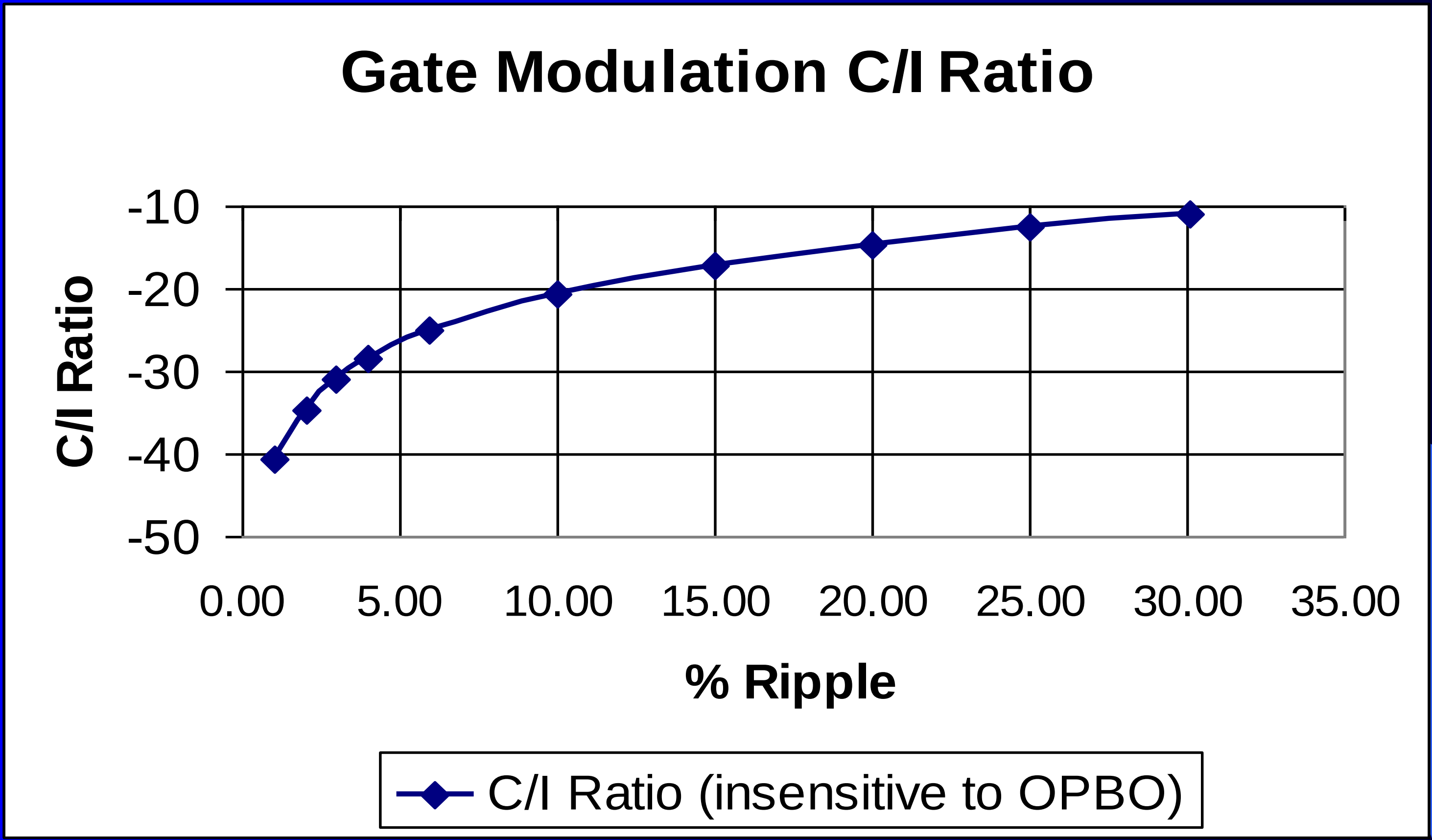
- Change in gate (or base) voltage can also be a significant contributor to memory effects
- This problem can be more difficult to solve than for the drain / collector case, and is quite different for BJT and FET devices
- PA stability can be a major concern
- Low currents are involved, so good power supply decoupling is easier to achieve
- GaAs FET gate supply must achieve good voltage regulation in spite of current flowing due to RF rectification by the gate-source diode

GATE MEMORY EFFECTS MINIMIZATION



The value of R* must be carefully chosen to provide a compromise between stability and bias-induced memory effects

GATE MEMORY EFFECTS



Measurement of the sensitivity of a GaAs FET PA to gate modulation

Ripple < 1% is required for C/I < 40 db

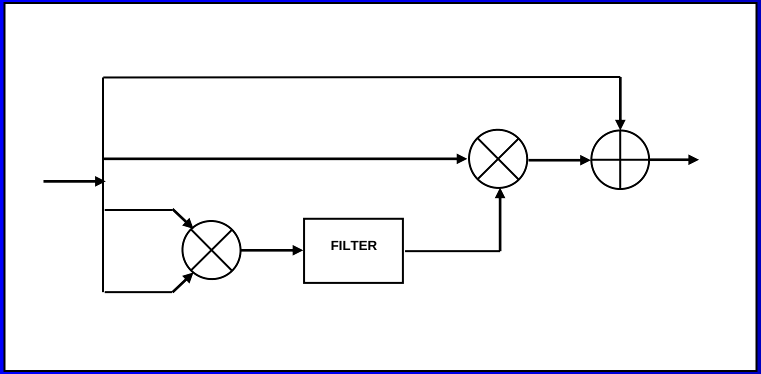
THERMAL MEMORY EFFECTS

- Major source of thermal memory effects is device junction temperature changes as a function of envelope frequency, particularly below 100 KHz
- Choice of device can minimize temperature memory effects. Temperature affects some devices less
- Bias class can also minimize temperature effects. Class A is less affected than class B, but has low efficiency
- Long term temperature changes (that do not depend on the envelope frequency) can also be considered a memory effect. Good thermal design or an adaptive circuitry can minimize this problem

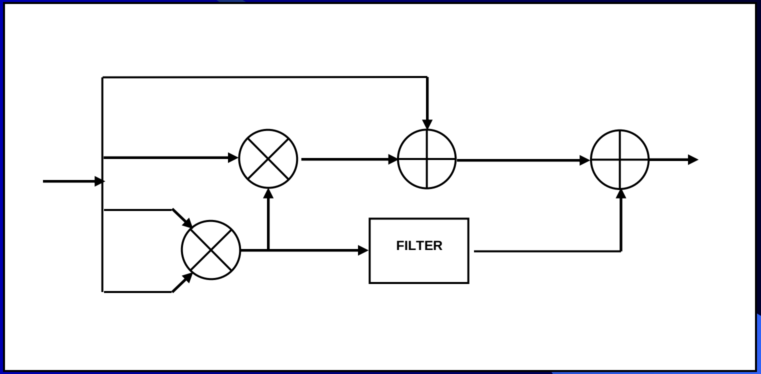
DEVICE RELATED MEMORY EFFECTS

- Some devices display changes in non-linear characteristics with envelope frequency that cannot be explained by bias modulation
- This phenomena appears related to current flow and charge trap build up. Some sources have attributed it to very small time-constant thermal effects
- Different devices show varying sensitivity. HBT, some LDMOS and GaN devices appear particularly sensitive
- No recommended solution except careful device selection

ADDITIONAL MEMORY EFFECTS CANCELLATION METHODS



Envelope Filtering



Envelope Injection

These methods are covered in the book “Distortion in RF Power Amplifiers” by J. Vuolevi and T. Rahkonen

Summary

- It is difficult to eliminate distortion caused by MEs using linearization
- Bias voltage variations (both drain/collector and gate/base) are a major cause of MEs
- Thermal change is another important source of MEs
- MEs can be minimized by careful electrical and mechanical design

Where to Get More Information

Vuolevi and Rahkonen, “Distortion in RF Power Amplifiers”, Artech House, 2003.

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